

1. A method of fabricating an integrated circuit device comprising:

depositing a composite etching stop layer overlying a substrate;

5 depositing a dielectric layer overlying said composite etching stop layer;

etching an opening through said dielectric layer stopping at said composite etching stop layer;

thereafter removing said composite etching stop
10 layer within said opening; and

filling said opening with a conducting layer to complete said fabrication of said integrated circuit device.

2. The method according to Claim 1 wherein said substrate comprises semiconductor device structures including gate electrodes and associated source and drain regions and metallization formed in and on a silicon substrate.

3. The method according to Claim 1 wherein said step of depositing said composite etching stop layer comprises:

depositing an etching stop layer selected from the group consisting of: silicon carbide, silicon nitride, SiCN, SiOC, SiOCN, and p-BCB; and

depositing a TEOS oxide layer by plasma-enhanced chemical vapor deposition overlying said etching stop layer.

4. The method according to Claim 1 wherein said composite etching stop layer has a thickness of between about 300 and 1000 Angstroms.

5. The method according to Claim 3 wherein said etching stop layer has a thickness of between about 200 and 600 Angstroms.

6. The method according to Claim 3 wherein said TEOS oxide layer has a thickness of between about 150 and 500 Angstroms.

7. The method according to Claim 3 wherein said TEOS oxide layer is deposited at less than about 450 °C.

8. The method according to Claim 1 wherein said dielectric layer is selected from the group consisting of: carbon-based silicate glass, polyarylene ethers, polyimides, and fluorine-doped silicate glass.

9. The method according to Claim 1 wherein said step of etching said opening through said oxide layer and said step of filling said opening comprises a damascene process.

10. A method of forming a composite etching stop layer comprising:

depositing an etching stop layer on a substrate wherein said etching stop layer is selected from the group consisting of: silicon carbide, silicon nitride,
5 SiCN, SiOC, SiOCN, and p-BCB; and

depositing a TEOS oxide layer by plasma-enhanced chemical vapor deposition overlying said etching stop layer.

11. The method according to Claim 10 wherein said substrate comprises semiconductor device structures including gate electrodes and associated source and drain regions formed in and on a silicon substrate.

12. The method according to Claim 10 wherein said composite etching stop layer has a thickness of between about 300 and 1000 Angstroms.

13. The method according to Claim 10 wherein said etching stop layer has a thickness of between about 200 and 600 Angstroms.

14. The method according to Claim 10 wherein said TEOS oxide layer has a thickness of between about 150 and 500 Angstroms.

15. The method according to Claim 10 wherein said TEOS oxide layer is deposited at less than about 450 °C.

16. The method according to Claim 10 further comprising:

depositing a dielectric layer overlying said composite etching stop layer;

etching an opening through said dielectric layer
5 stopping said at composite etching stop layer;

thereafter removing said composite etching stop layer within said opening; and

filling said opening with a conducting layer to complete fabrication of an integrated circuit device.

17. The method according to Claim 16 wherein said dielectric layer is selected from the group consisting of: carbon-based silicate glass, polyarylene ethers, polyimides, and fluorine-doped silicate glass.

18. The method according to Claim 16 wherein said step of etching said opening through said oxide layer and said step of filling said opening comprises a damascene process.

19. A method of fabricating an integrated circuit device comprising:

depositing a composite etching stop layer overlying a substrate wherein said depositing comprises:

5 depositing an etching stop layer selected from the group consisting of: silicon carbide, silicon nitride, SiCN, SiOC, SiOCN, and p-BCB; and

 depositing a TEOS oxide layer by plasma-enhanced chemical vapor deposition overlying said
10 etching stop layer;

 depositing a dielectric layer overlying said composite etching stop layer;

 etching an opening through said dielectric layer stopping at said composite etching stop layer;

15 thereafter removing said composite etching stop layer within said opening; and

 filling said opening with a conducting layer to complete said fabrication of said integrated circuit device.

20. The method according to Claim 19 wherein said substrate comprises semiconductor device structures including gate electrodes and associated source and drain regions formed in and on a silicon substrate.

21. The method according to Claim 19 wherein said composite etching stop layer has a thickness of between about 300 and 1000 Angstroms.

22. The method according to Claim 19 wherein said etching stop layer has a thickness of between about 200 and 600 Angstroms.

23. The method according to Claim 19 wherein said TEOS oxide layer has a thickness of between about 150 and 500 Angstroms.

24. The method according to Claim 19 wherein said TEOS oxide layer is deposited at less than about 450 °C.

25. The method according to Claim 19 wherein said dielectric layer is selected from the group consisting of: carbon-based silicate glass, polyarylene ethers, polyimides, and fluorine-doped silicate glass.

26. The method according to Claim 19 wherein said step of etching said opening through said oxide layer and said step of filling said opening comprises a damascene process.